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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,980	05/24/2001	Peter Aymar	GR 00 P 1969	3471

24131 7590 09/12/2005

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EXAMINER	
ALPHONSE, FRITZ	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/864,980	AYMAR ET AL.	
	Examiner	Art Unit	
	Fritz Alphonse	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-31,33,39 and 44-49* is/are rejected.

7)☒ Claim(s) *32,34-38 and 40-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 49 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 49 recites the limitation "The method according to claim 44, which further comprises: storing a respective state metric, which is stored in the initial state register, of the initial state of the trellis in a respective buffer register as soon as a final state has been read from a final state register; and ". It seems that the claim is incomplete. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 22-31, 39, 44-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina (U.S. Pat. No. 5,987,490) in view of Kong (U.S. Pat. No. 6,029,268).

As to claim 22, Alidina (fig.3) shows an apparatus for executing a Viterbi algorithm, including: initial state registers (i.e., register 34; col. 4, lines 42-64) each storing a state metric of an initial state of a trellis having a butterfly structure (col. 5, lines 19-32), a state metric (col. 2,

lines 50-59), and a transition metric (col. 2, lines 12-24); at least one transition register storing the transition metric of the trellis (i.e.; registers 46); evaluation units (col. 6, lines 42-50). Alidina (fig. 3) shows an adder/subtracter network (32) for processing signals, said adder/subtracter network (32) connected: to said initial state registers (34); to said at least one transition register (46); and to said evaluation units in accordance with the butterfly structure of the trellis; said evaluation units evaluating signals processed by said adder/subtracter network in accordance with a Viterbi algorithm (col. 6, lines 19-29); a selection unit (see figure 4) switching the apparatus between first and second operating modes (col. 7, lines 26-42).

Alidina does not explicitly disclose a final state registers connected to evaluation units. However. In the same field of endeavor, Kong discloses a quality calculator apparatus for use with Viterbi-decoded data, wherein a final states registers are used for storing the state metric of a respective final state of the trellis (col. 1, lines 49-53).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Alidina with the apparatus, as disclosed by Kong. Doing so would provide a quality calculator apparatus for use with Viterbi-decoded data, in which zero-state metrics of demodulated data input to a Viterbi-decoder, are used as parameters for the quality evaluation in order to calculate the quality of the decoded data (col. 1, lines 32-37).

As to claims 23-25, Alidina (fig. 3) shows an apparatus, wherein at least one of said initial state registers (34) has a buffer register (discrete registers and X and Y registers); and, wherein said at least one transition register at least one of stores a transition metric when said selection unit switches the apparatus to said first operating mode (col. 4, lines 47-50); and stores a change transition metric when said selection unit switches the apparatus to said second

operating mode (col. 4, lines 50-65). Alidina teaches that said at least one transition register stores a transition metric when said selection unit switches the apparatus to said first operating mode (col. 2, lines 12-24); and stores a change transition metric when said selection unit switches the apparatus to said second operating mode (col. 6, lines 30-50).

As to claims 26-28, and 29-31, Alidina (fig. 3) shows an apparatus, wherein said at least one transition register is storing at least two transition registers to two different transition metrics when said selection unit switches the apparatus to said second operating mode (col. 8, lines 5-11). The apparatus includes a signal bus (42) connected to said initial state registers, said at least one transition register (34), and said final state registers (46); and a processor connected to said initial state registers, said at least one transition register, and said final state registers through said signal bus, wherein said processor is programmed to calculate the state metric and the transition metric (col. 4, lines 42-50).

As to claim 39, Alidina (figs. 3, 4) discloses an apparatus, wherein the selection unit includes a selection register and at least one multiplexer is connected to said selection unit (col. 6, lines 3-12).

As to claim 44, method claim 44 corresponds to apparatus claim 22; therefore, it is analyzed as previously discussed in claim 22 above.

As to claims 45-47, Alidina (fig. 3) discloses a method comprises using the Viterbi algorithm to process physical signals (col. 6, lines 51 through col. 7 line 9). The method comprises using the Viterbi algorithm to equalize and decode received physical signals dependent upon the selected one of the operating modes, and decode received physical signals in

a first of the operating modes and to equalize the received physical signals in a second of the operating modes (col. 8, lines 5-11).

As to claims 48-49, Alidina discloses a method comprises decoding physical signals in a first of the operating modes; and equalizing the physical signals in a second of the operating modes (col. 7, lines 59 through col. 8 line 11). The method further comprises storing a respective state metric, which is stored in the initial state register, of the initial state of the trellis in a respective buffer register as soon as a final state has been read from a final state register (col. 1, lines 49-53).

4. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina in view of Kong as applied to claim 22 above, and further in view of Park (U.S. Pat. No. 5,446,746).

As to claim 33, Alidina does not explicitly disclose evaluation units include at least one of: a trace-back register. However, this is obvious and very well known in the art, as evidenced by Park (fig. 11; col. 6, lines 16-25).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to improve upon the path memory, as disclosed by Park. Doing so would provide a path memory apparatus of Viterbi decoder, which has a simple structure resulting in a reduced size, which can be implemented in a semiconductor integrated circuit (col. 1, lines 55-60).

Allowable Subject Matter

5. Claims 32, 34-38, 40-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3824.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fritz Alphonse

Art Unit 2133

August 30, 2005

GUY LAMARRE
PRIMARY EXAMINER